

Design and Verification of an HDR-DDR Enabled I3C Master Controller Using Verilog

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Abstract— Reliable and high-speed data communication is increasingly important in modern embedded systems and System-on-Chip (SoC) architectures, where multiple peripheral devices operate through a shared communication bus. Although the conventional Inter-Integrated Circuit (I2C) interface offers a simple and widely adopted solution, its limited transfer rate restricts its suitability for applications requiring higher communication throughput. The Inter-Integrated Circuit (I3C) standard addresses these limitations by providing enhanced data transfer performance along with features such as dynamic addressing, in-band interrupts, and backward compatibility with I2C devices. This work presents the design and functional verification of an I3C Master Controller incorporating High Data Rate–Double Data Rate (HDR-DDR) communication using Verilog HDL. The proposed design is organized into dedicated modules for clock generation, protocol control using a finite state machine, frame generation, HDR-DDR data transmission, data reception, and bus interfacing. In HDR-DDR mode, data is transferred on both rising and falling transitions of the clock, allowing two data transfers within a single clock cycle without requiring an increase in the operating clock frequency. The controller was simulated, functionally verified, and synthesized using the Xilinx Vivado design environment to evaluate its operational correctness and hardware implementation feasibility. The obtained results demonstrate that the proposed architecture can support efficient I3C communication while maintaining a modular and scalable structure. The design can serve as a suitable foundation for FPGA-based embedded communication systems and can be further extended for hardware optimization and future ASIC implementation.

Keywords— I3C, HDR-DDR, Verilog HDL, I3C Master Controller, High-Speed Serial Communication, Embedded Systems, Finite State Machine (FSM), Functional Verification.

I. INTRODUCTION

The continuous growth of embedded computing has increased the need for communication interfaces capable of exchanging

information quickly and reliably among processing units and peripheral devices. Applications such as industrial automation, automotive electronics, smart sensors, healthcare equipment, and Internet of Things (IoT) platforms require communication protocols that can handle larger data volumes while maintaining stable operation and efficient hardware utilization. Consequently, communication performance has become a key factor in the design of modern digital systems.

For many years, the Inter-Integrated Circuit (I2C) protocol has served as a practical solution for short-distance serial communication because of its simple two-wire interface and straightforward implementation. Despite its popularity, the protocol encounters performance limitations when used in systems containing numerous high-speed peripherals. Restricted bandwidth and increasing communication overhead reduce its effectiveness in applications where rapid and continuous data exchange is required.

To satisfy these emerging requirements, the Improved Inter-Integrated Circuit (I3C) protocol was introduced as an enhanced communication standard. The protocol retains interoperability with compatible I2C devices while incorporating features that improve bus efficiency and communication flexibility. Support for dynamic address assignment, efficient interrupt handling, and optimized data transfer enables I3C to meet the requirements of current embedded platforms with greater communication efficiency.

Among the operating modes available in I3C, High Data Rate–Double Data Rate (HDR-DDR) provides a practical approach for increasing communication throughput. Instead of transferring information on only one clock transition, HDR-DDR utilizes both the positive and negative clock edges to transmit successive data bits. This technique increases the amount of data communicated during each clock cycle without requiring a higher clock frequency, making it suitable for applications that demand improved communication performance.

In this work, an HDR-DDR enabled I3C Master Controller is designed using Verilog Hardware Description Language (HDL). The proposed architecture is organized into functional modules including clock generation, frame generation, finite state machine (FSM) control, HDR-DDR transmission logic,

receiver logic, and bus interface circuitry. Functional verification and synthesis are carried out using the Xilinx Vivado development environment to validate the behavior of the controller and assess its implementation feasibility. The resulting architecture provides a structured and scalable communication controller that can be integrated into FPGA-based embedded systems and further extended for future ASIC development.

II. BACKGROUND

A. CONVENTIONAL I2C PROTOCOL

Communication between digital components is a fundamental requirement in embedded system design. Among the available serial interfaces, the Inter-Integrated Circuit (I2C) protocol has gained wide acceptance because it provides communication through only two signal lines, namely the Serial Clock (SCL) and Serial Data (SDA). A controller initiates communication by selecting the destination device through its address, after which data is exchanged in a synchronized manner. The straightforward hardware structure and the ability to connect multiple peripherals on the same bus have made I2C suitable for numerous embedded applications.

As embedded platforms have become more sophisticated, communication traffic has increased considerably. Under these conditions, the limited transfer capability of I2C affects overall system efficiency, particularly when several intelligent peripherals must exchange information within strict timing requirements.

B. EVOLUTION TO THE I3C

To meet the communication demands of modern electronic systems, the Improved Inter-Integrated Circuit (I3C) protocol was introduced as an enhanced serial interface. The protocol retains interoperability with compatible legacy devices while extending communication capability through additional protocol features. These enhancements improve bus efficiency, simplify device management, and support faster information exchange between the controller and connected peripherals.

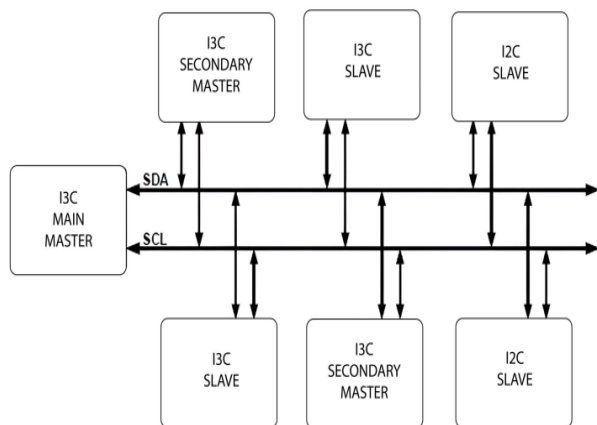


Figure 1. I3C Protocol

The architectural improvements of I3C allow it to serve applications where communication performance is a critical design factor, including sensor networks, portable electronics, industrial equipment, and automotive control systems.

C. HDR-DDR DATA TRANSFER

One of the performance-oriented operating modes supported by I3C is High Data Rate–Double Data Rate (HDR-DDR). HDR-DDR operation improves transmission efficiency by utilizing both positive and negative clock edges for data movement. This approach enables two data transfers within one clock cycle, increasing effective throughput without requiring an increase in clock frequency.

D. FPGA-BASED DESIGN APPROACH

Digital communication controllers are commonly verified on FPGA platforms before ASIC realization because FPGA devices provide flexibility for design validation and performance evaluation. Hardware behavior can be analyzed through functional simulation, synthesis, and timing analysis before physical implementation.

In this work, the proposed HDR-DDR enabled I3C Master Controller is developed using Verilog HDL and synthesized with Xilinx Vivado. The implementation is functionally verified through simulation, and synthesis reports are examined to study hardware utilization and timing performance.

E. NEED FOR THE PROPOSED DESIGN

Emerging embedded applications require communication interfaces that combine high throughput with efficient hardware implementation. Existing low-speed serial interfaces cannot always satisfy these requirements. The proposed HDR-DDR enabled I3C Master Controller addresses this need by employing double-edge data transmission within an FPGA-based architecture, enabling improved communication performance while maintaining an efficient digital design.

III. METHODOLOGY

The implementation procedure involves designing an I3C master controller architecture with HDR-DDR capability using Verilog HDL. A modular development strategy is followed, where individual hardware blocks are designed separately and integrated through FSM-based coordination to achieve complete protocol functionality.

A. SYSTEM ARCHITECTURE

The proposed architecture consists of multiple hardware modules that cooperate to execute an I3C communication transaction. The primary modules include the clock generation unit, finite state machine (FSM), frame generation logic, HDR-DDR transmitter, receiver, and bus interface. These modules communicate through internal control and data signals to ensure synchronized operation.

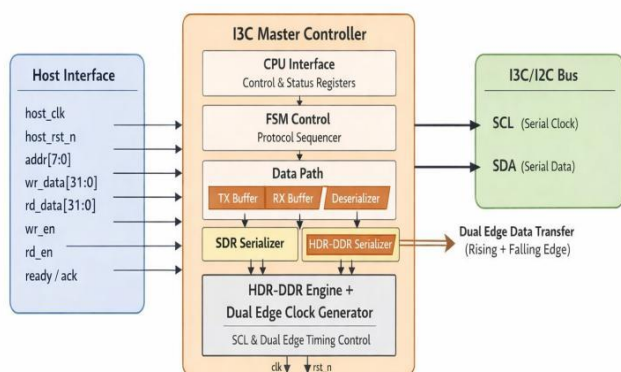


Figure 2. HDR-DDR Enabled I3C Master Controller

The communication process begins when the master controller receives a request to initiate a transaction. The clock generation unit produces the required timing signals, after which the FSM activates the frame generation logic. The generated frame contains the control information, device address, command field, and data payload required for communication. During data transmission, the HDR-DDR transmitter serializes the parallel input data and transfers it through the SDA line. Simultaneously, the receiver monitors the incoming serial data and reconstructs it into parallel format whenever data reception is required. After successful completion of the communication sequence, the FSM returns the controller to the idle state, making it ready for the next transaction.

The modular organization improves readability of the hardware design, simplifies debugging, and allows individual modules to be verified independently before complete system integration.

A. CLOCK GENERATION

Reliable communication requires accurate timing signals. Therefore, the proposed controller incorporates a dedicated clock generation module responsible for producing the clock required for I3C communication. The generated clock maintains synchronization between the transmitter and receiver throughout the communication process.

During HDR-DDR operation, both transitions of the clock signal are utilized for data transfer. The clock generation module therefore provides stable rising and falling edges with uniform timing characteristics. This enables consecutive data bits to be transmitted within a single clock cycle, increasing communication efficiency without increasing the operating frequency.

The generated clock is distributed to all functional modules, ensuring synchronized execution of state transitions, address transmission, command generation, and data transfer. Proper clock management also contributes to reliable protocol execution during functional verification.

B. FINITE STATE MACHINE

The Finite State Machine (FSM) functions as the central controller of the proposed architecture. It supervises every

stage of protocol execution by controlling the sequence of operations performed by each hardware module.

Initially, the FSM enters the Idle state, where it waits for a communication request. After receiving a start signal, the controller moves to the Initialization state and activates the clock generation module. The FSM then proceeds to Address Transmission, where the target device address is placed on the communication bus. Following successful address transmission, the controller enters the Command state to transmit the selected communication command.

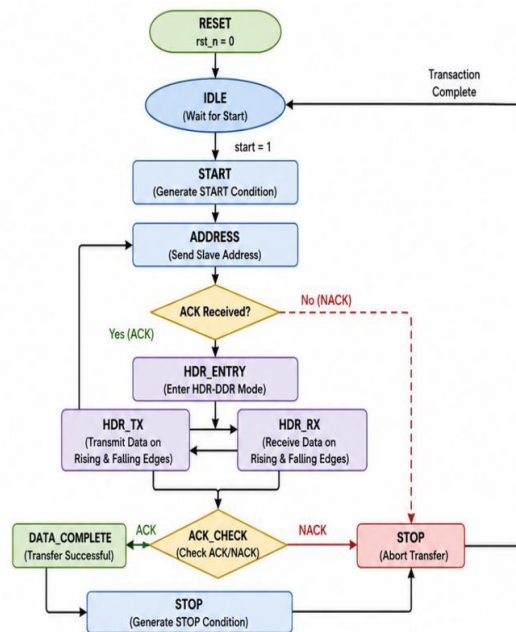


Figure 3. Finite State Machine

Once the command phase is completed, the FSM activates the HDR-DDR transmission module to perform high-speed data transfer. Throughout this stage, the FSM continuously monitors completion signals generated by the transmitter and receiver modules. After all data bits have been transferred successfully, the controller generates the required stop condition and returns to the Idle state, preparing the system for the next communication cycle.

The FSM-based control strategy ensures that every protocol operation is executed in the correct sequence while preventing timing conflicts between individual hardware modules.

C. HDR-DDR TRANSMISSION

The HDR-DDR transmission module represents the key contribution of the proposed controller. Unlike conventional single-edge communication, this module transfers information during both the rising and falling transitions of the clock signal. Consequently, two data bits can be transmitted within a single clock period, effectively increasing communication throughput without increasing clock frequency.

The transmitter first converts parallel input data into serial format before placing individual bits onto the SDA line. One

bit is transmitted during the positive clock transition, while the following bit is transmitted during the negative transition. The receiver samples the incoming data using the corresponding clock edges and reconstructs the original parallel information.

This double-edge transmission mechanism improves bus utilization and allows higher communication efficiency while maintaining protocol reliability. The modular implementation also enables future enhancements such as error detection, CRC generation, and additional HDR operating modes without significant architectural modification.

D. FUNCTIONAL VERIFICATION

Functional verification is performed to ensure that every module operates according to the intended design specification. The complete controller is simulated using Xilinx Vivado, where individual hardware modules are integrated into a single top-level design. A dedicated Verilog testbench generates clock, reset, control, and data signals required to evaluate controller operation.

Simulation waveforms are analyzed to verify system initialization, FSM state transitions, address transmission, command execution, HDR-DDR data transfer, and transaction completion. Correct synchronization between the clock generation module, transmitter, receiver, and FSM confirms the successful execution of the communication protocol.

After functional verification, the design is synthesized using Xilinx Vivado to obtain hardware implementation statistics, including Look-Up Table (LUT) utilization, Flip-Flop (FF) usage, timing information, and estimated power consumption. These synthesis results demonstrate the feasibility of implementing the proposed architecture on FPGA devices and provide an assessment of hardware efficiency.

IV. RESULTS AND DISCUSSIONS

The proposed HDR-DDR enabled I3C Master Controller was designed using Verilog HDL and verified in the Xilinx Vivado environment. The correctness of the proposed architecture was evaluated through RTL schematic generation and functional simulation. These results confirm that the developed controller performs the intended communication sequence and supports HDR-DDR data transmission.

A. RTL SCHEMATIC

The RTL schematic shown in Figure 4 represents the synthesized hardware architecture of the proposed controller. The generated schematic confirms that the design has been successfully translated into interconnected hardware modules including the clock generation unit, finite state machine (FSM), frame generation logic, HDR-DDR transmitter, receiver, and bus interface.

The RTL implementation demonstrates a modular architecture in which each functional block performs a dedicated task while communicating through well-defined control and data paths. Such an organization improves design readability, simplifies debugging, and enables individual module verification before complete system integration.

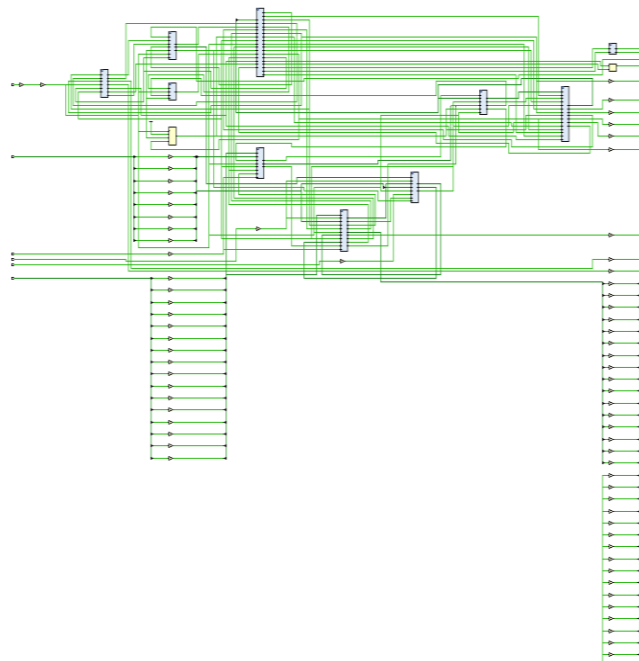


Figure 4. RTL Schematic Of HDR-DDR I3C Master Controller

The absence of disconnected signals or undefined logic in the synthesized schematic indicates that the hardware description is structurally complete. Furthermore, the modular architecture facilitates future enhancements, allowing additional protocol features to be incorporated without major architectural modifications. This confirms that the proposed design provides a scalable implementation suitable for FPGA realization.

B. SIMULATION RESULTS

Figure 5 presents the functional simulation waveform of the proposed HDR-DDR enabled I3C Master Controller. The waveform verifies the successful execution of the communication sequence under different operating conditions generated by the Verilog testbench.

Initially, the active-low reset initializes the controller and places the finite state machine in the idle state. After the reset is released, the write enable signal initiates a communication request, allowing the input data to be loaded into the transmission path. The finite state machine then progresses through the required protocol states while coordinating frame generation, address transmission, command execution, and HDR-DDR data transfer.

The waveform confirms that the Serial Clock (SCL) and Serial Data (SDA) signals remain synchronized throughout the communication cycle, demonstrating correct protocol timing. Debug signals associated with the HDR-DDR transmission further verify that data bits are processed on both the rising and falling edges of the clock. The assertion of the HDR mode activation and transmission enable signals confirms successful switching from the initialization phase to high-speed HDR-DDR communication.



Figure 5. Functional Simulation Waveform of the HDR-DDR Enabled I3C Master Controller.

Unlike conventional SDR communication, where only one data bit is transferred during each clock cycle, the proposed implementation performs data transmission on both clock transitions. This double-edge transmission mechanism increases the effective data throughput without increasing the operating clock frequency. Consequently, the proposed architecture improves communication efficiency while maintaining stable protocol timing.

The simulation also demonstrates correct interaction among the clock generation module, FSM, frame generation logic, transmitter, receiver, and bus interface. No unexpected state transitions, invalid timing relationships, or communication failures were observed during simulation. These observations confirm that the proposed controller satisfies the intended functional requirements and can reliably support high-speed I3C communication.

C. SYNTHESIS RESULTS

After functional verification, the proposed controller was synthesized using Xilinx Vivado 2025.2 to evaluate its hardware implementation characteristics. The synthesis results indicate that the design satisfies all timing constraints and can be successfully implemented on the selected FPGA device.

The power analysis report indicates a total on-chip power consumption of 0.435 W, consisting of 0.338 W dynamic power and 0.097 W static power. The relatively low dynamic power demonstrates that the proposed HDR-DDR communication mechanism can achieve higher communication performance without introducing excessive power overhead.

The implementation report further shows that the clock network, routing resources, logic elements, and input/output interfaces collectively contribute to the overall power consumption. Among these components, the I/O circuitry exhibits the highest switching activity because continuous serial communication occurs through the SDA and SCL lines during HDR-DDR transmission. Despite this increased communication activity, the overall power consumption remains within acceptable limits for FPGA-based embedded applications.

The implementation also operates within the recommended thermal limits, with a junction temperature of approximately 26.1°C, indicating stable hardware operation under the evaluated conditions. The successful timing closure further confirms that all setup and hold timing requirements are satisfied, ensuring reliable operation of the controller at the target clock frequency.

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.454 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.1°C
Thermal Margin: 58.9°C (24.0 W)
Ambient Temperature: 25.0 °C
Effective θ JA: 2.4°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

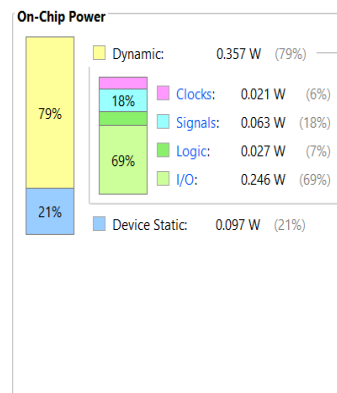


Figure 6. Power Analysis Report of the Proposed HDR-DDR Enabled I3C Master Controller.

Overall, the synthesis results demonstrate that the proposed architecture achieves a balanced trade-off between communication performance and hardware efficiency. The combination of low power consumption, successful timing closure, and modular architecture makes the proposed HDR-DDR enabled I3C Master Controller suitable for high-speed embedded communication systems and provides a strong foundation for future ASIC implementation.

V. CONCLUSIONS AND FUTURE SCOPE

This research demonstrated the FPGA-based realization of an HDR-DDR supported I3C master controller using Verilog HDL. The developed architecture successfully integrates communication control, data transmission, and verification modules. Simulation and synthesis results confirm that the proposed design achieves reliable operation with efficient resource utilization and acceptable power performance. The implementation successfully satisfied the timing requirements while utilizing FPGA resources efficiently and achieving a total on-chip power consumption of 0.435 W. These results demonstrate that the proposed controller is a suitable solution for FPGA-based embedded communication applications.

Future work will focus on hardware validation using an FPGA development board and the integration of advanced I3C features such as In-Band Interrupt (IBI), Hot-Join, and Common Command Codes (CCC). Further optimization for reduced resource utilization, lower power consumption, and ASIC implementation can also be explored to support next-generation embedded and IoT systems.



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